

Asus Radeon RX Vega 64 ROG-STRIX-RXVEGA64-O8G-GAMING D050PIL Rev 1.00X

1. Vega10 PCBs Edge Connector

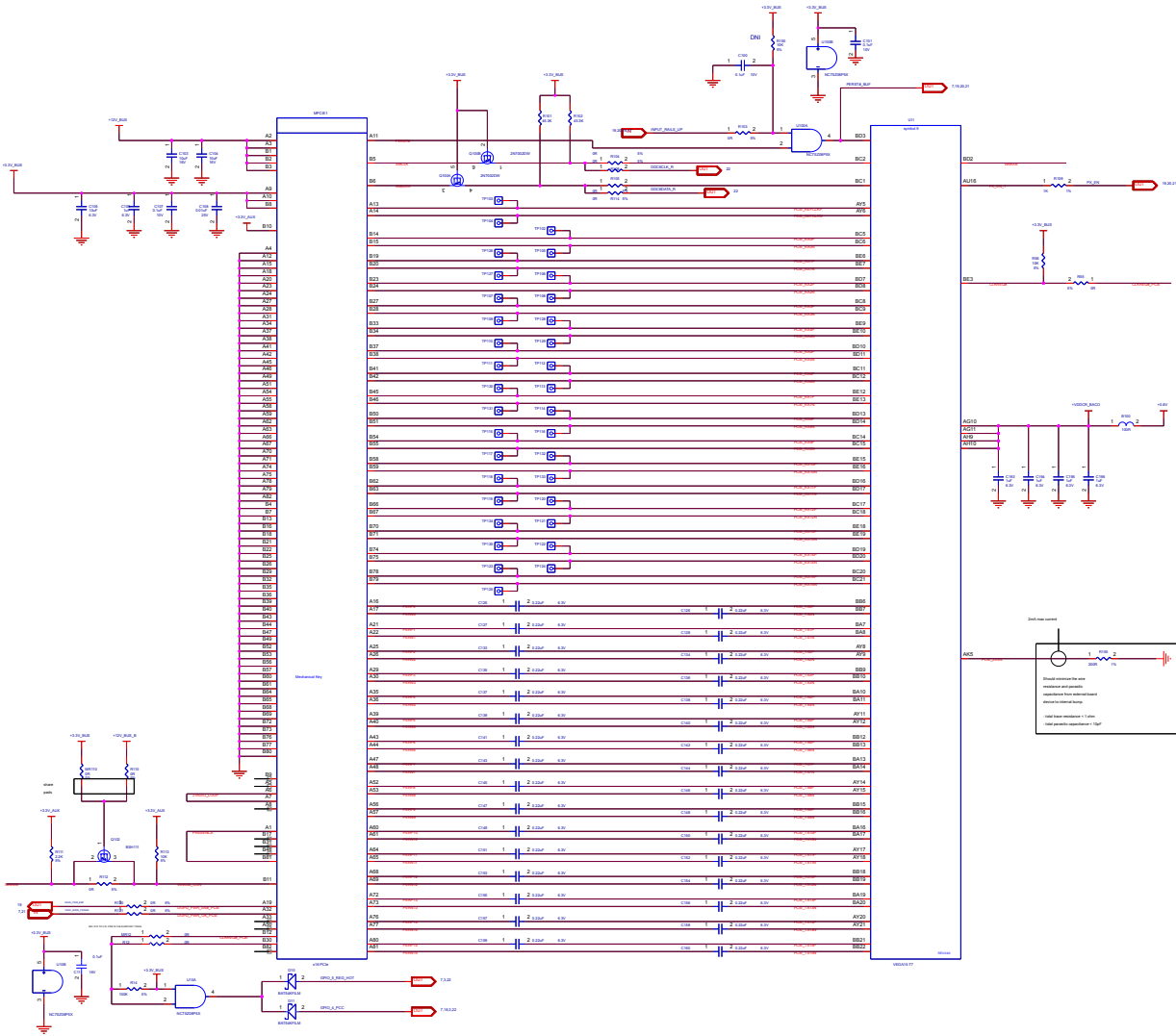
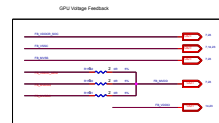
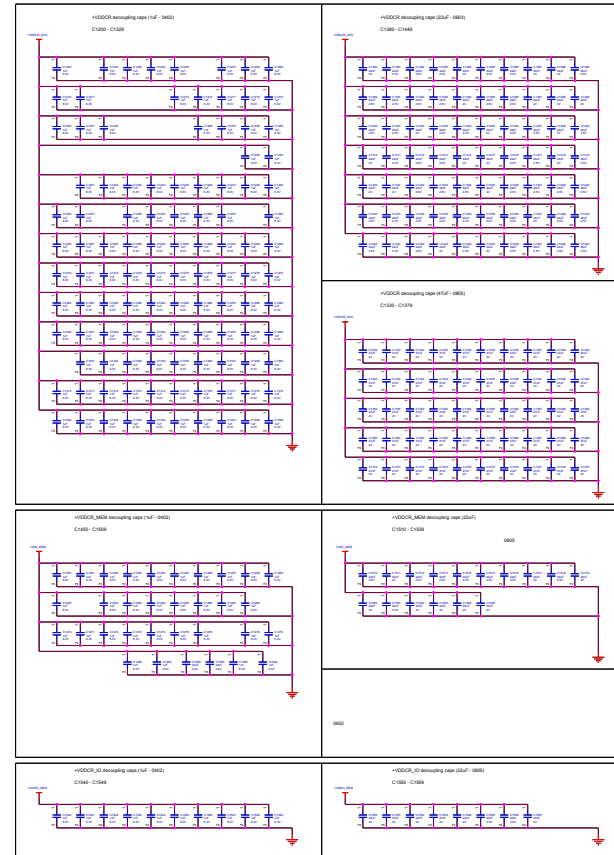
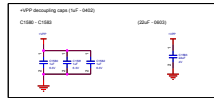
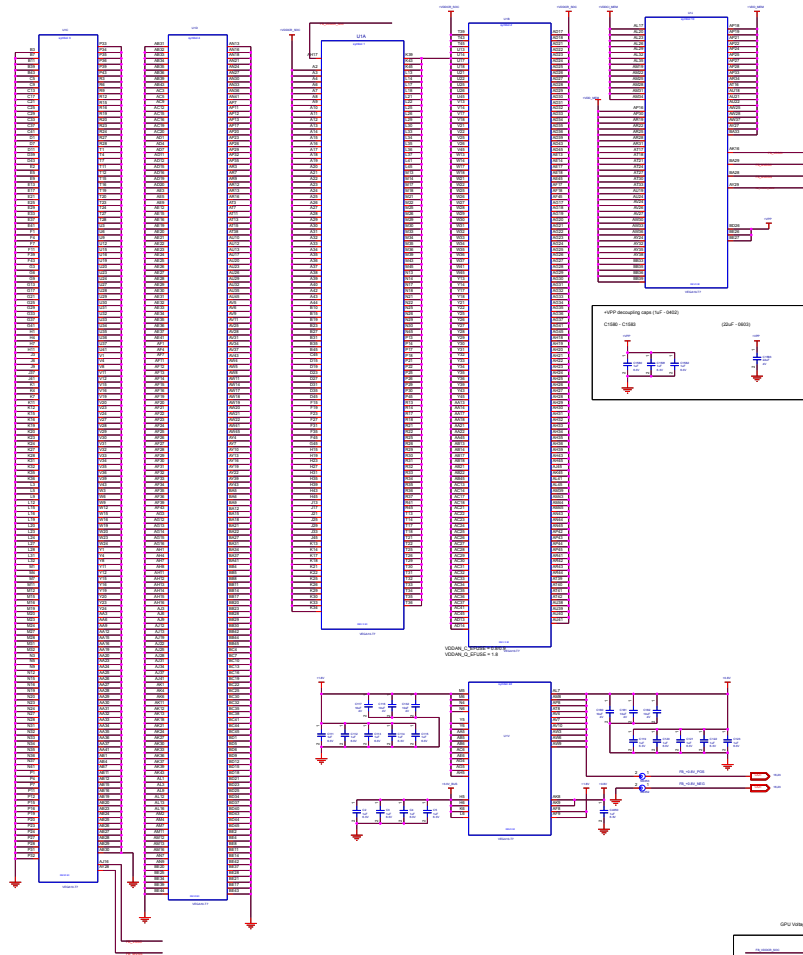


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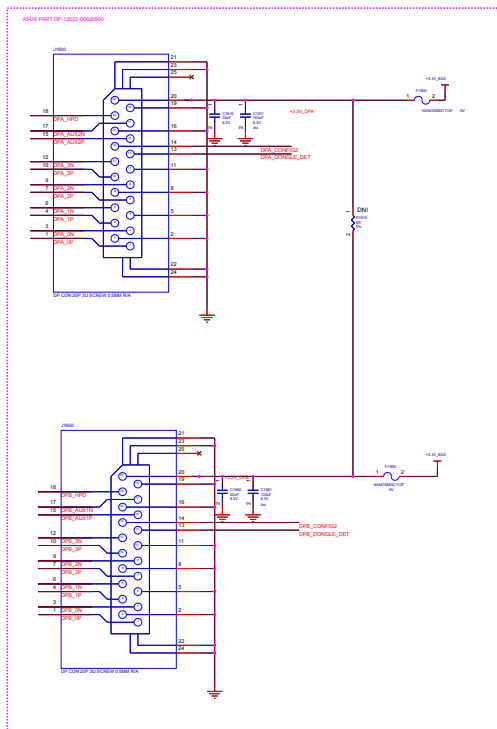
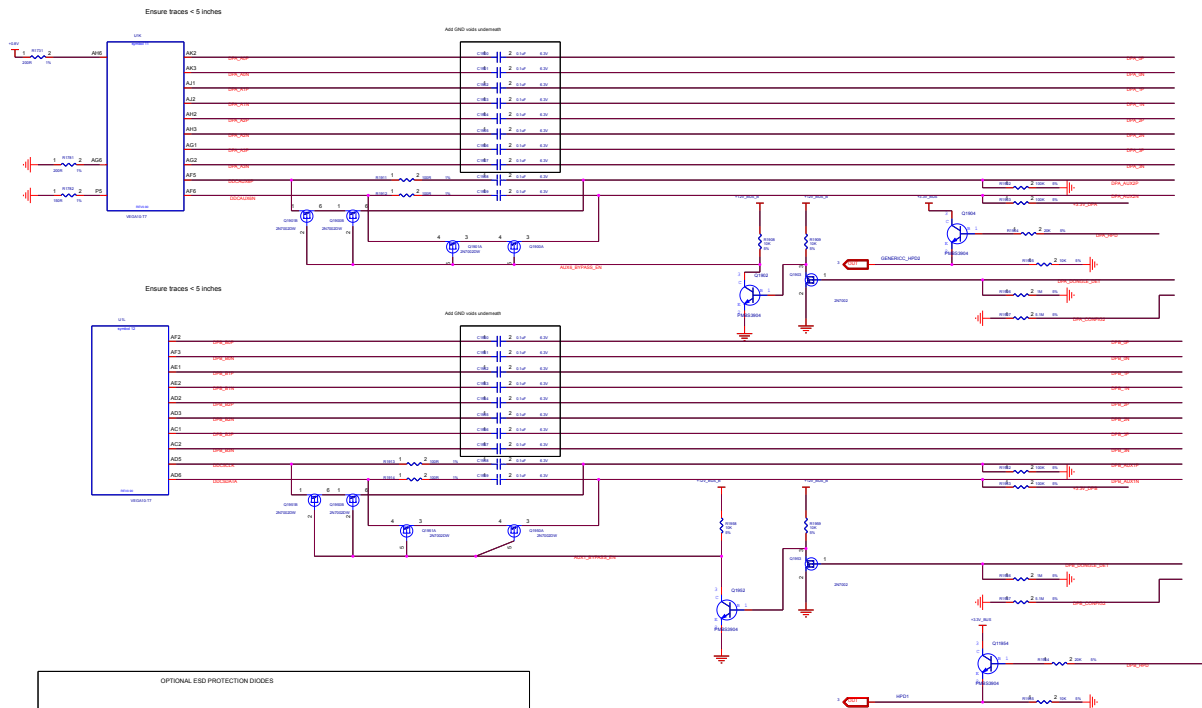
SHEET NO.	SHEET NAME
1	Vega10 - PCBs Interface
2	Vega10 - Power 1 GND
3	Vega10 - OPTIO EXTRA
4	Vega10 - OPTIO FREE, VPM, DAP, DRAMCANNON
5	Vega10 - THERMAL TADP, THERMAL & +5V VESA
6	Vega10 - THERMAL TADP
7	Control - VDDIO, VDDIO2
8	Reg - VDDIO, VDDIO2 PHASES 1 and 2
9	Reg - VDDIO, VDDIO2 PHASES 3 and 4
10	Reg - VDDIO, VDDIO2 PHASES 5 and 6
11	Reg - VDDIO, VDDIO2 PHASES 7 and 8
12	Reg - VDDIO, VDDIO2 PHASES 9 and 10
13	Reg - VDDIO, VDDIO2 PHASES 11 and 12
14	Reg - VDDIO, VDDIO2
15	Reg - VDDIO, VDDIO2 and VPM
16	Reg - VDDIO
17	Reg - VDDIO, VDDIO2
18	PCD - VDDIO
19	POWER MANAGEMENT
20	THERMAL
21	GPU/IO & BACKLIGHT
22	DEBUG
23	PI BLUE
24	BLOCK DIAGRAM
25	REVISION HISTORY



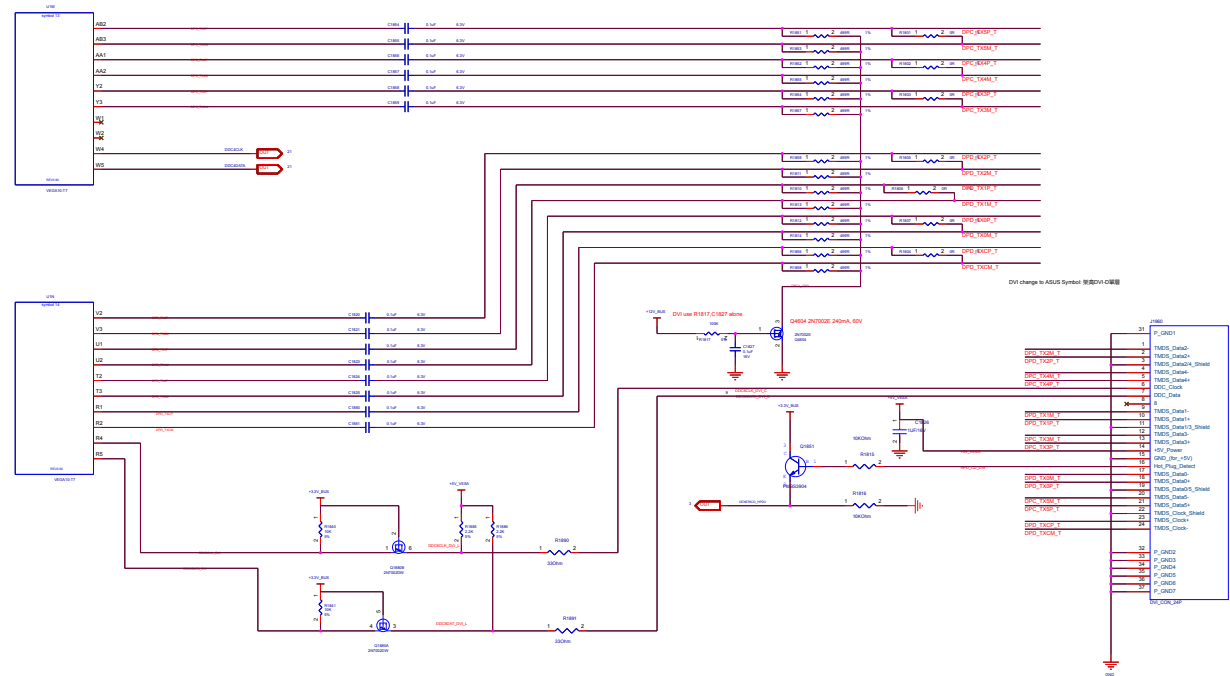
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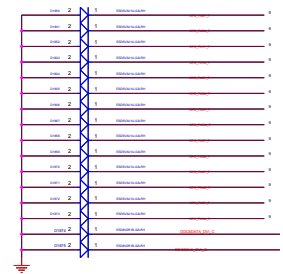
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A200	A200		



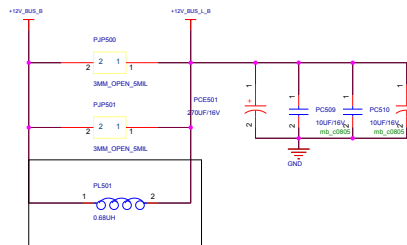
(9) ELLESMERE TMDPAB dDVI



OPTIONAL ESD PROTECTION DIODES

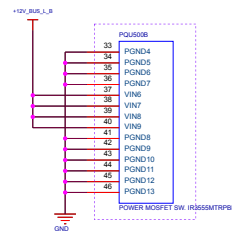
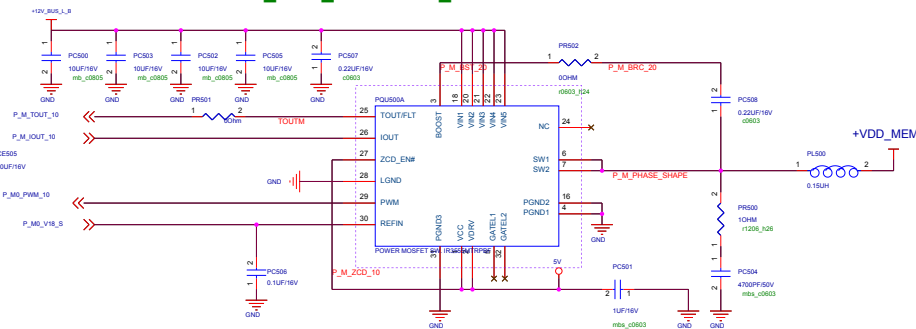


Tripple=6.3A
I_{in}=2.815A

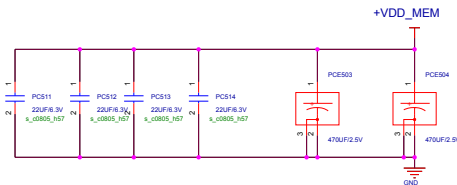


改09016-00330700>0.33uH

+12V_BUS_B -> +VDD_MEM

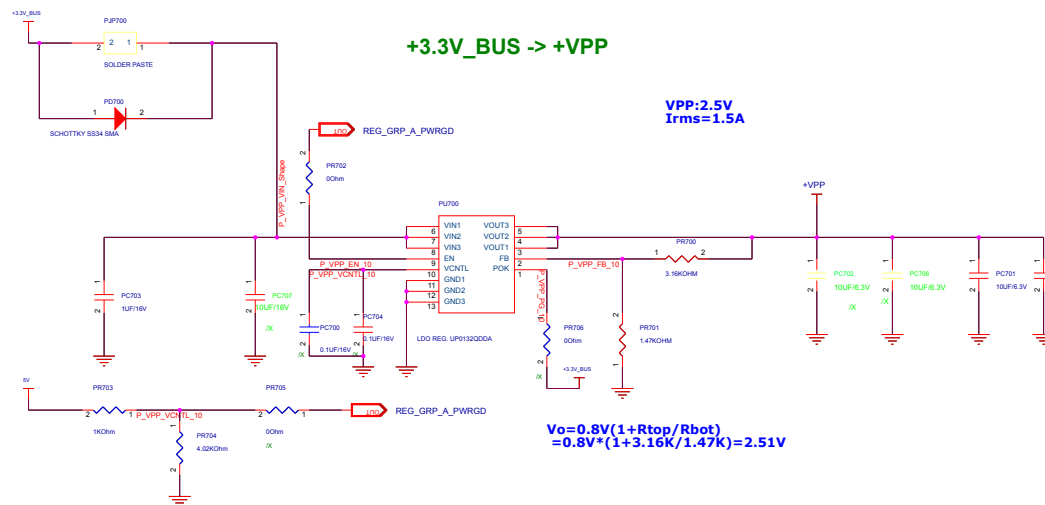


+VDD_MEM:1.35V
I_{out}=20A



+3.3V_BUS -> +VPP

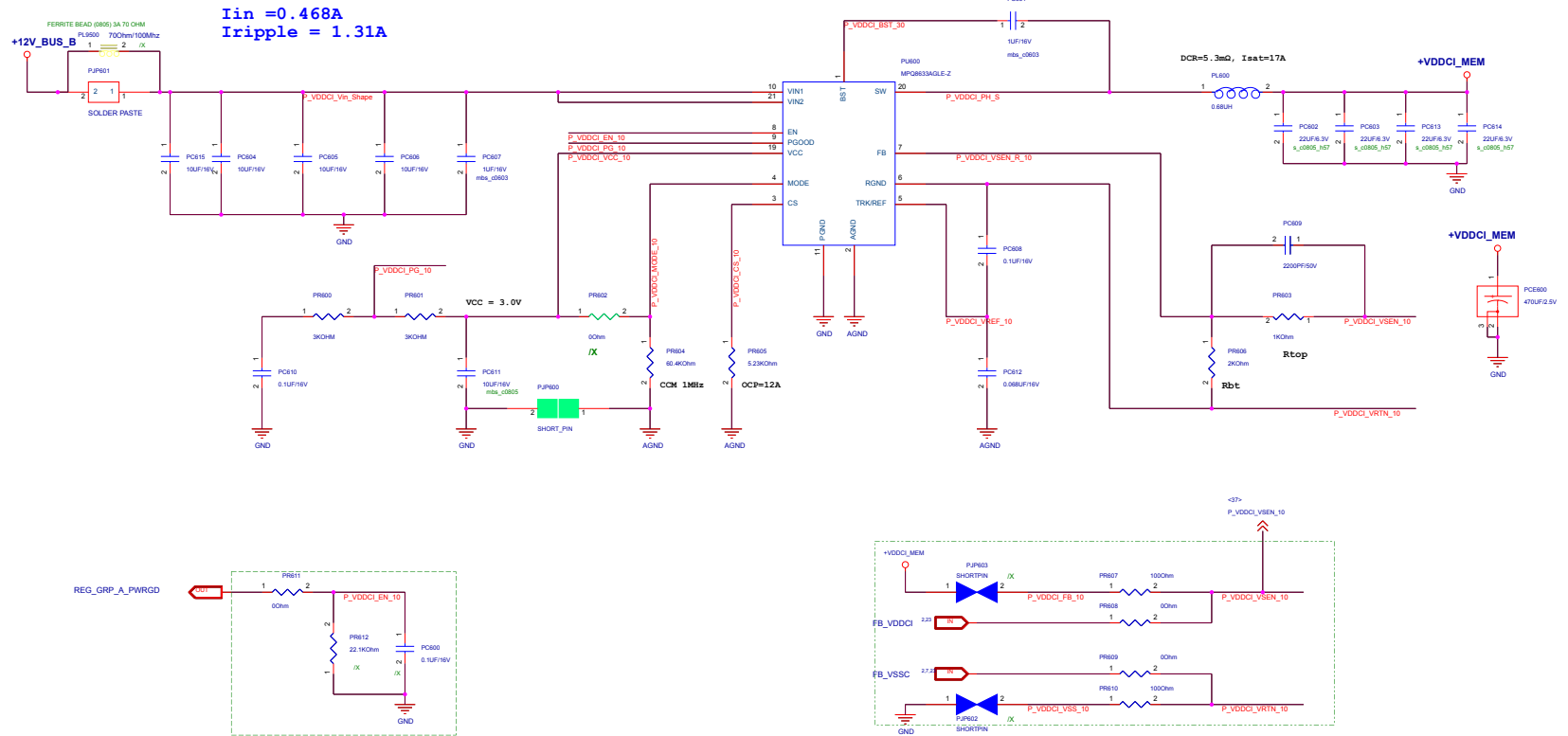
VPP:2.5V
I_{rms}=1.5A



$$V_o = 0.8V \cdot (1 + R_{top}/R_{bot}) = 0.8V \cdot (1 + 3.16K/1.47K) = 2.51V$$

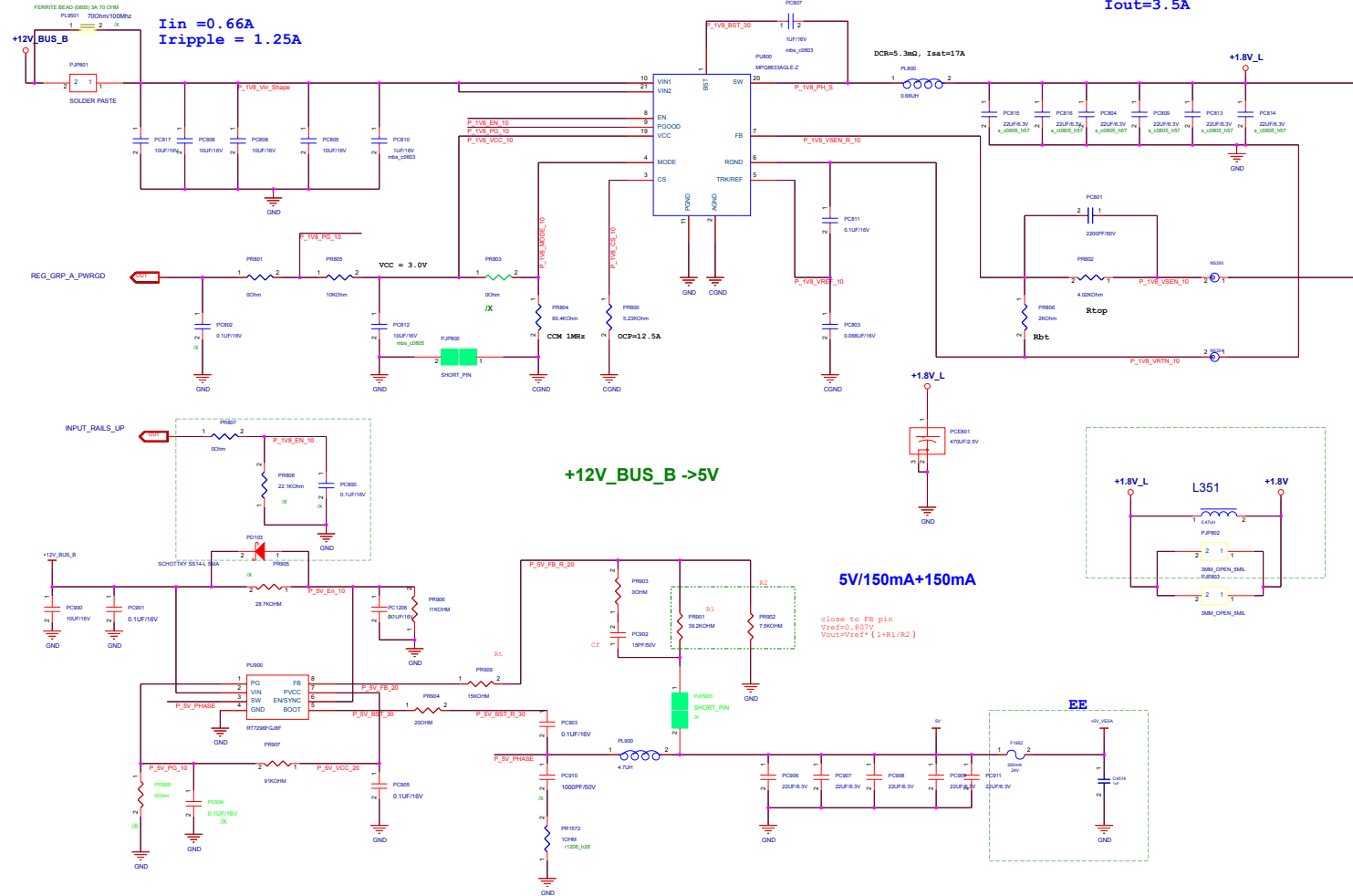
+12V_BUS_B -> +VDDCI_MEM

0.9V
I_{out}=5A



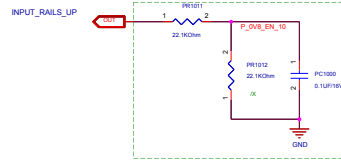
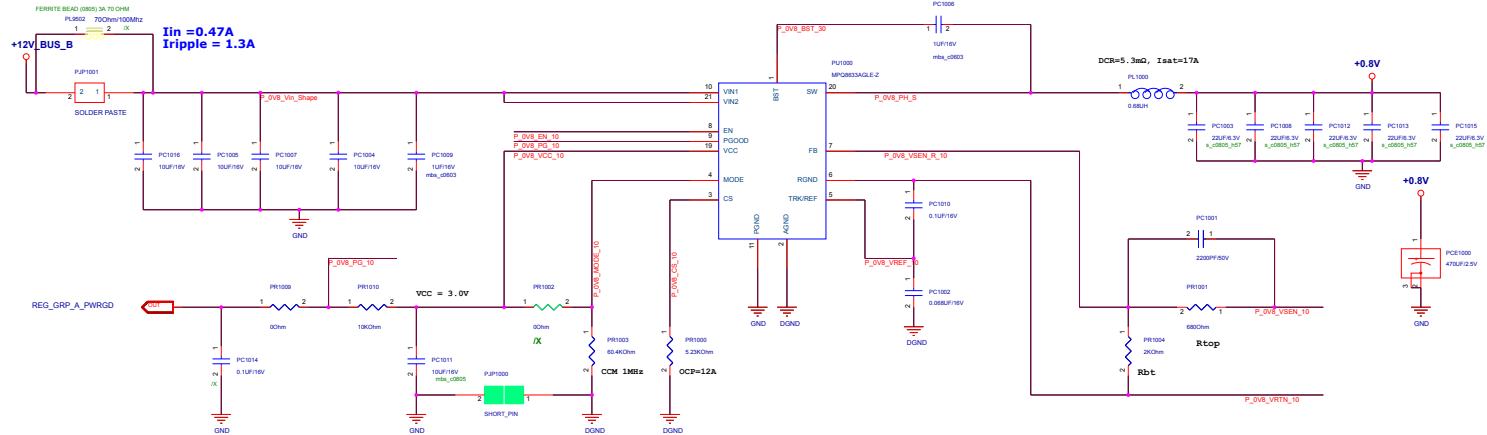
+12V_BUS_B ->+1.8V

+1.8V
I_{out}=3.5A



+12V_BUS_B->0.8V

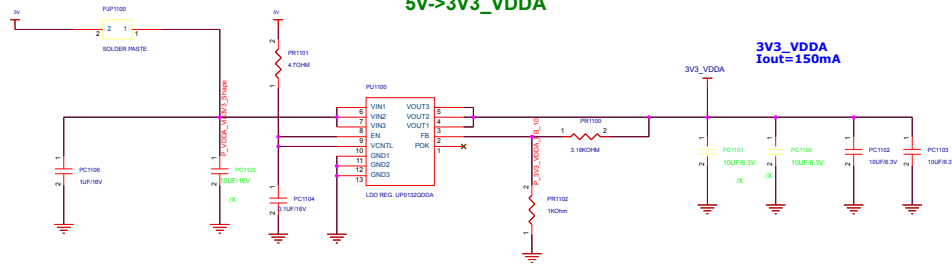
+0.9V
I_{out}=5A



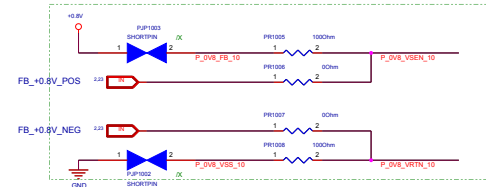
delay:2.24ms

5V->3V3_VDDA

3V3_VDDA
I_{out}=150mA



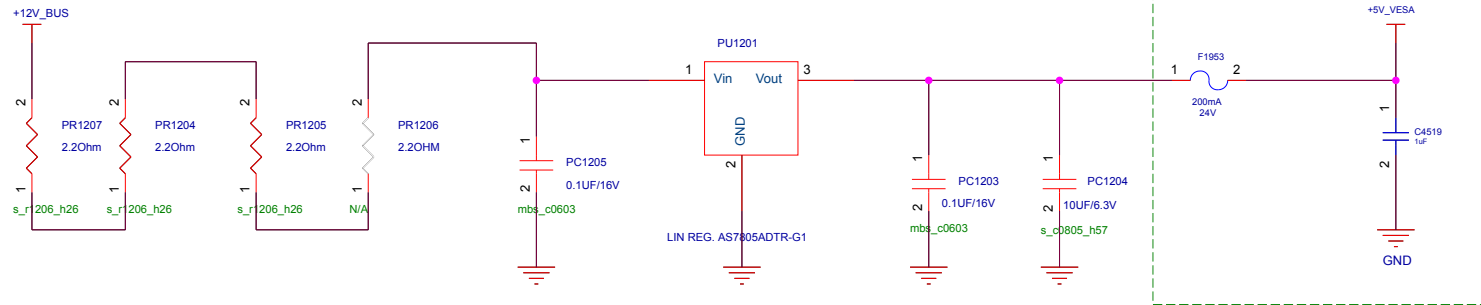
$$V_o = 0.8V \cdot (1 + R_{top}/R_{bot}) = 0.8V \cdot (1 + 3.16k/1.47k) = 2.51V$$

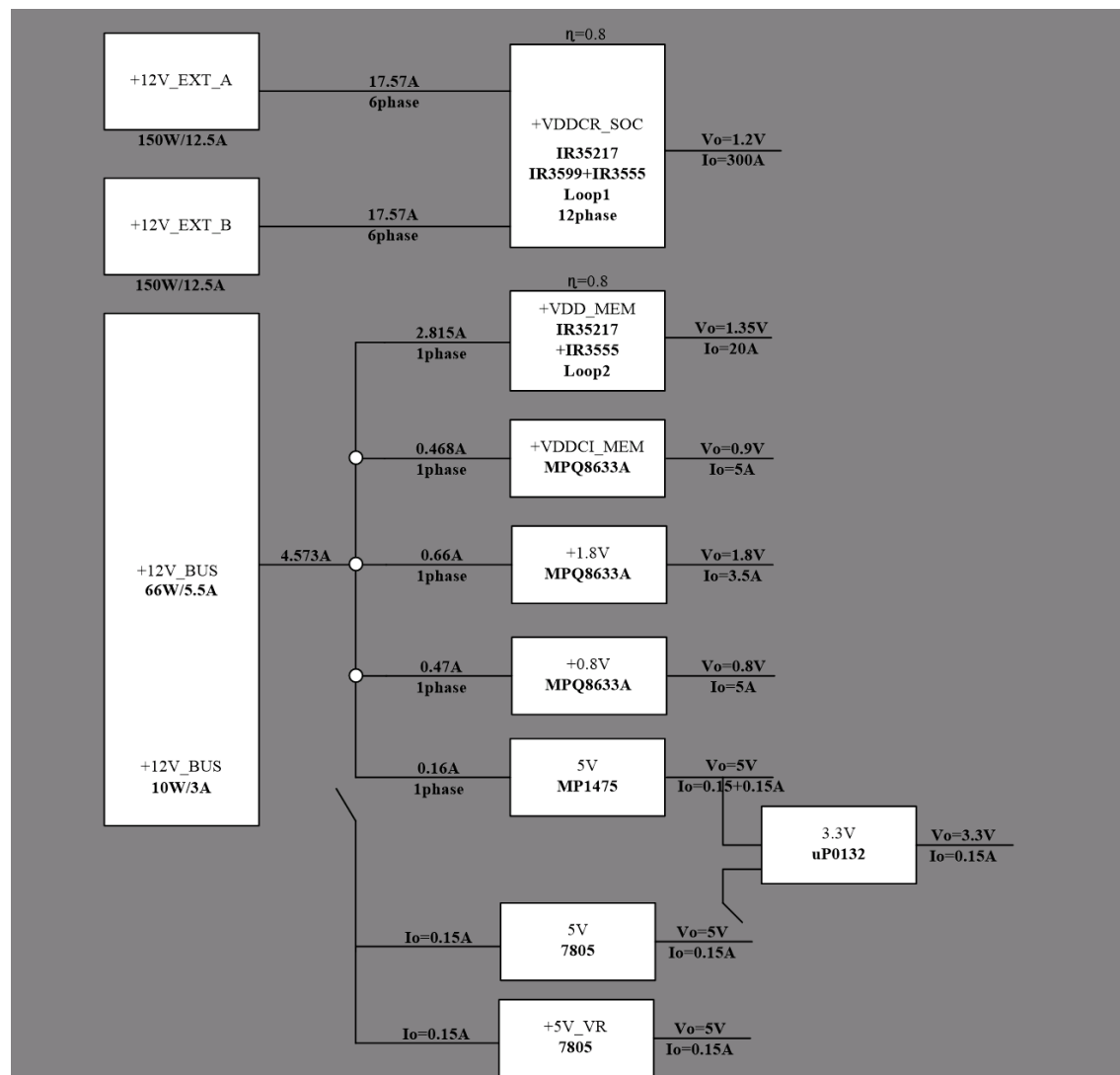


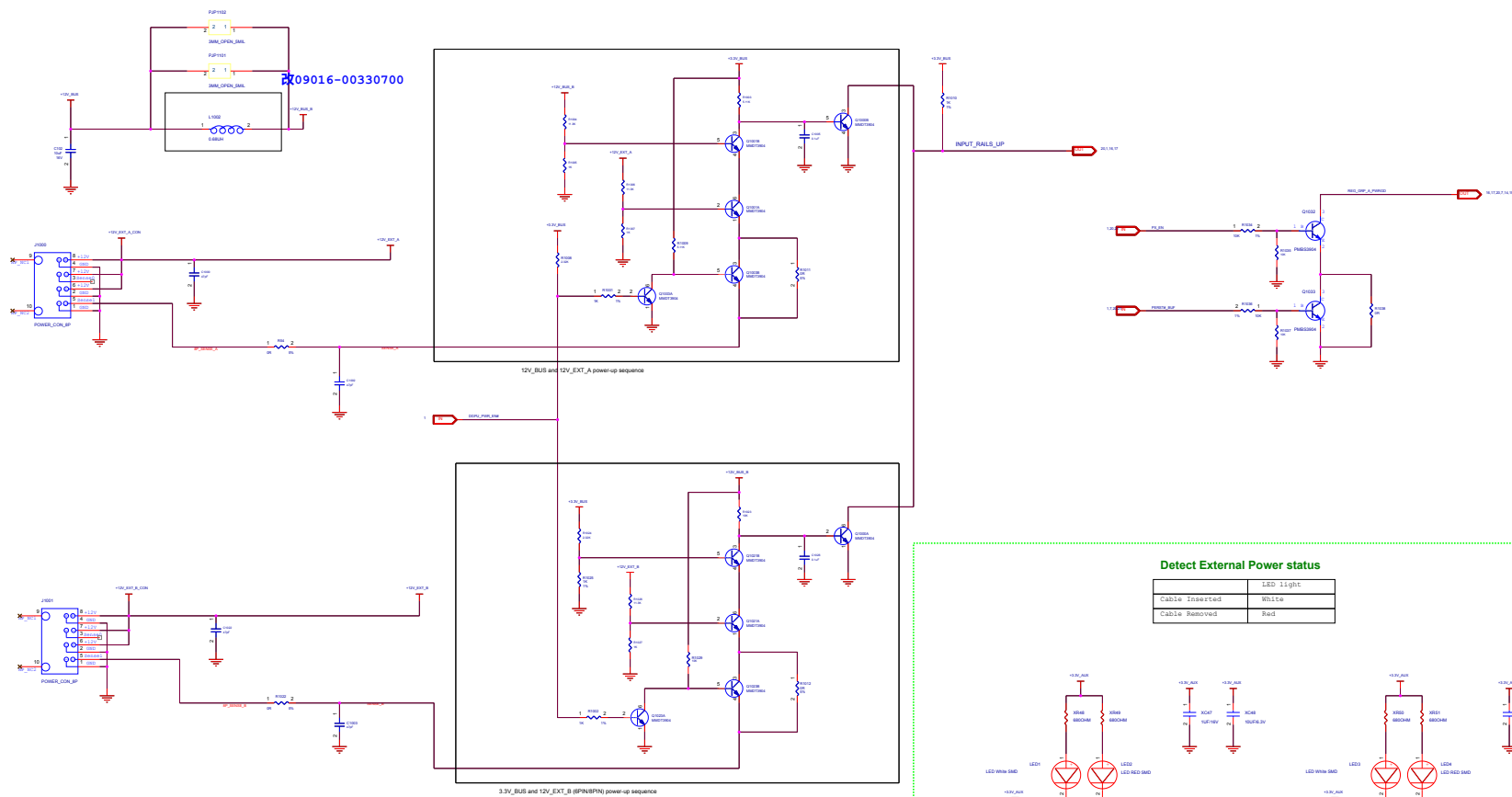
12V_BUS --> +5V

5V/150mA

EE

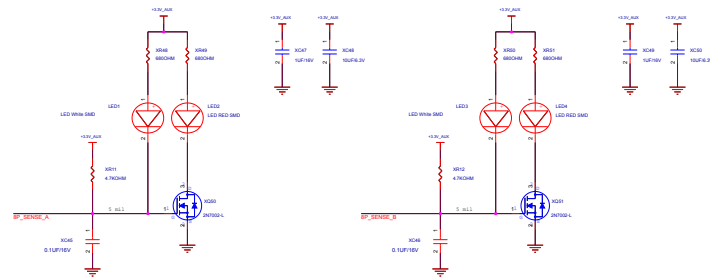


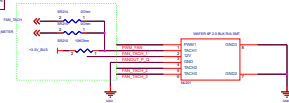




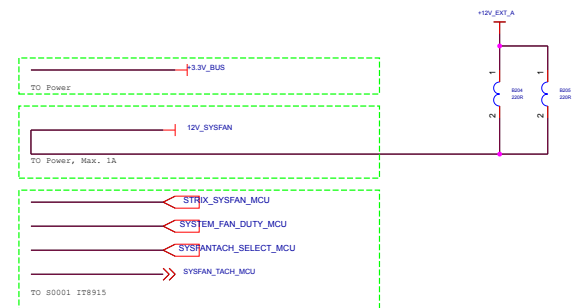
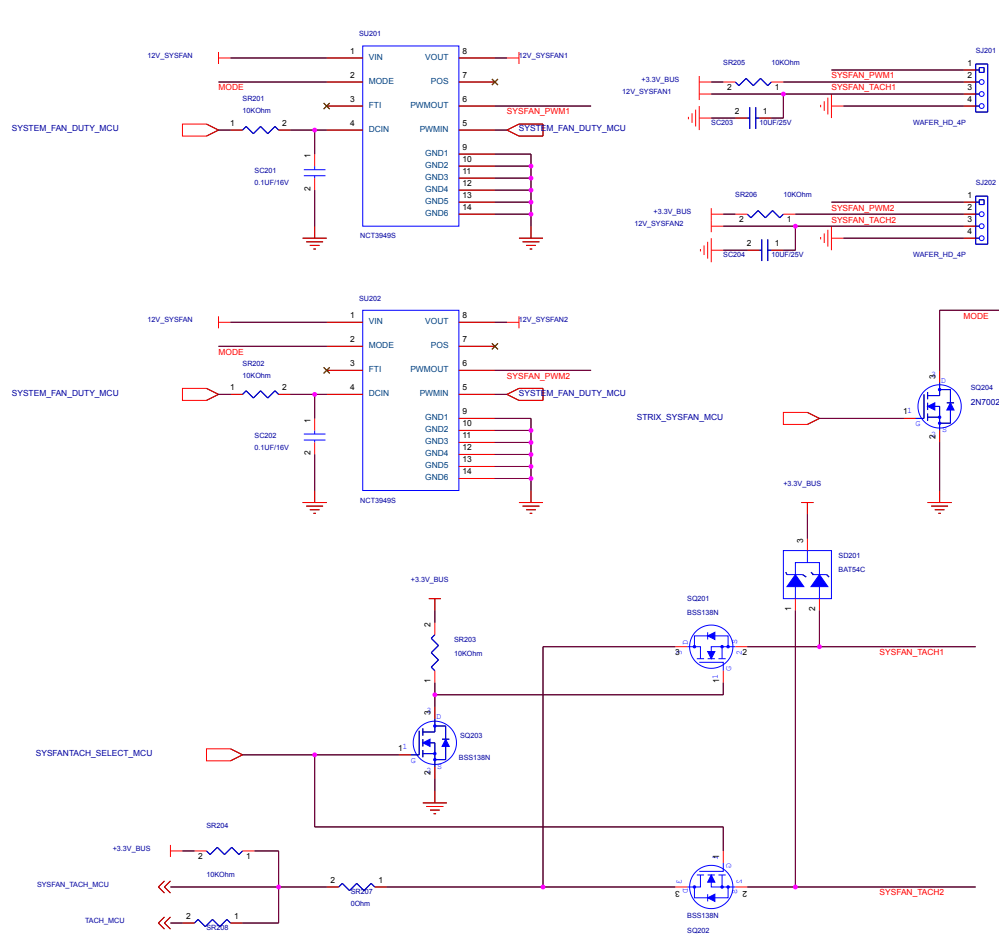
Detect External Power status

	LED: Light
Cable: Inserted	Blue
Cable: Removed	Red

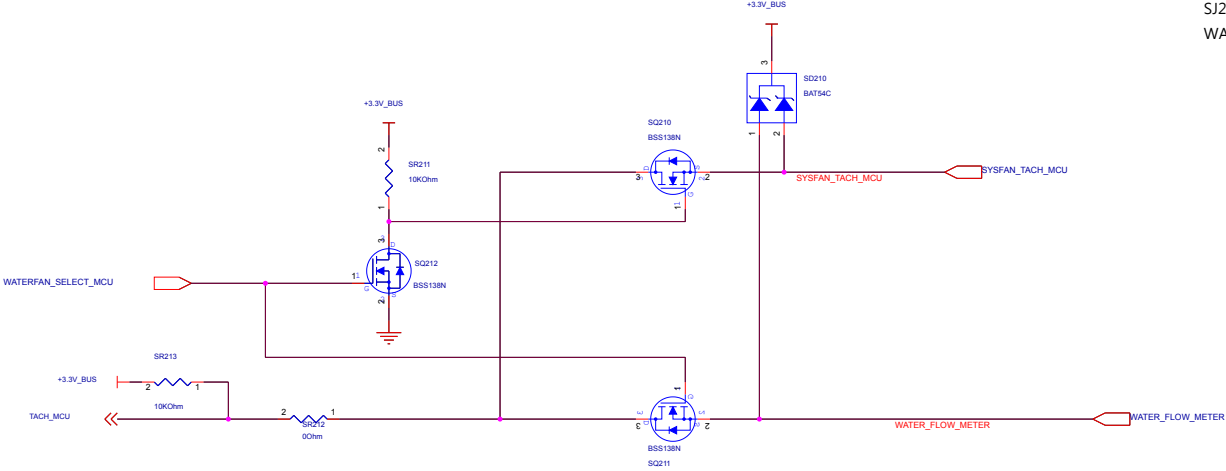
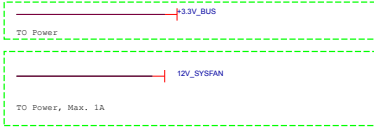






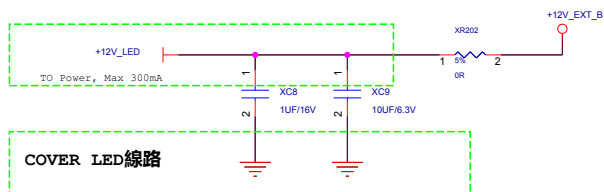
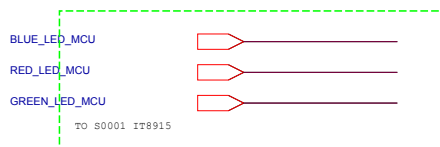
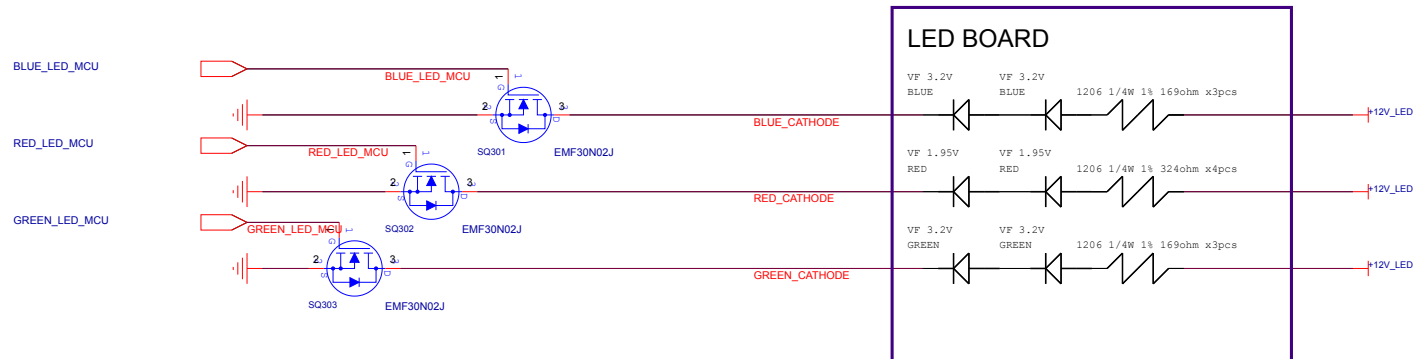


STRIX_SYSFAN_MCU	Mode
L	NORMAL
H(Default)	STRIX
SYSFANTACH_SELECT_MCU	Mode
L	SYSFAN_TACH1
H(Default)	SYSFAN_TACH2



SJ210 可與VGA Card Fan Conn共用
SJ210 所使用之12V_SYSFAN 可更改為原設計VGA Card之12V
WATER_FLOW_METER若需變更Net Name須注意應拉到的Net

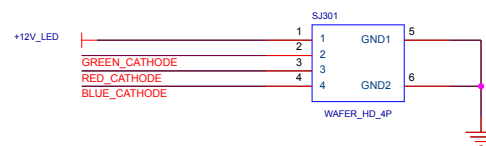
SYSFANTACH_SELECT_MCU	Mode
L	SYSFAN
H (Default)	WATER FLOW METER

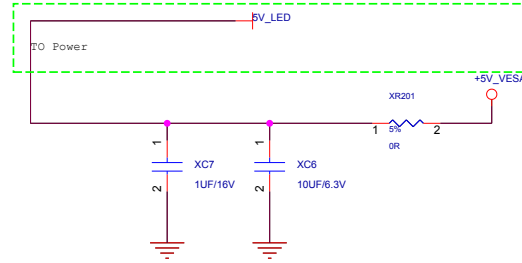


示意圖

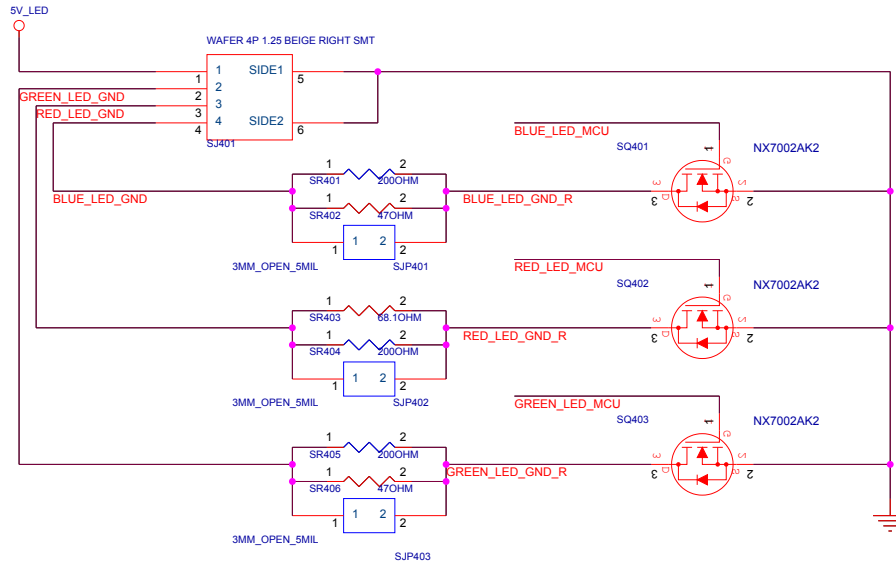


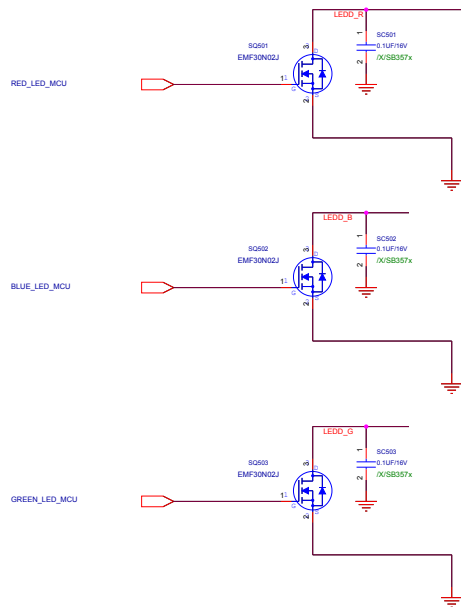
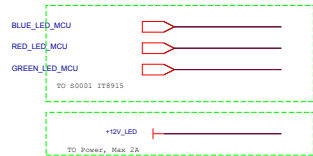
連接座旁請註明 12V G R B





背板ROG LED線路





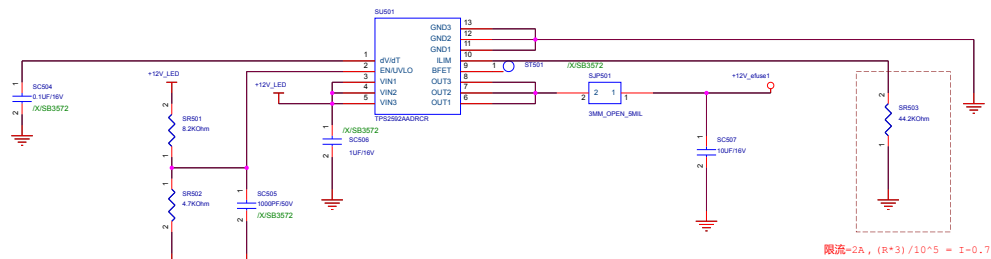
示意图



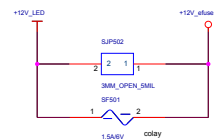
连接座旁请註明 12V G R B
RGB Header

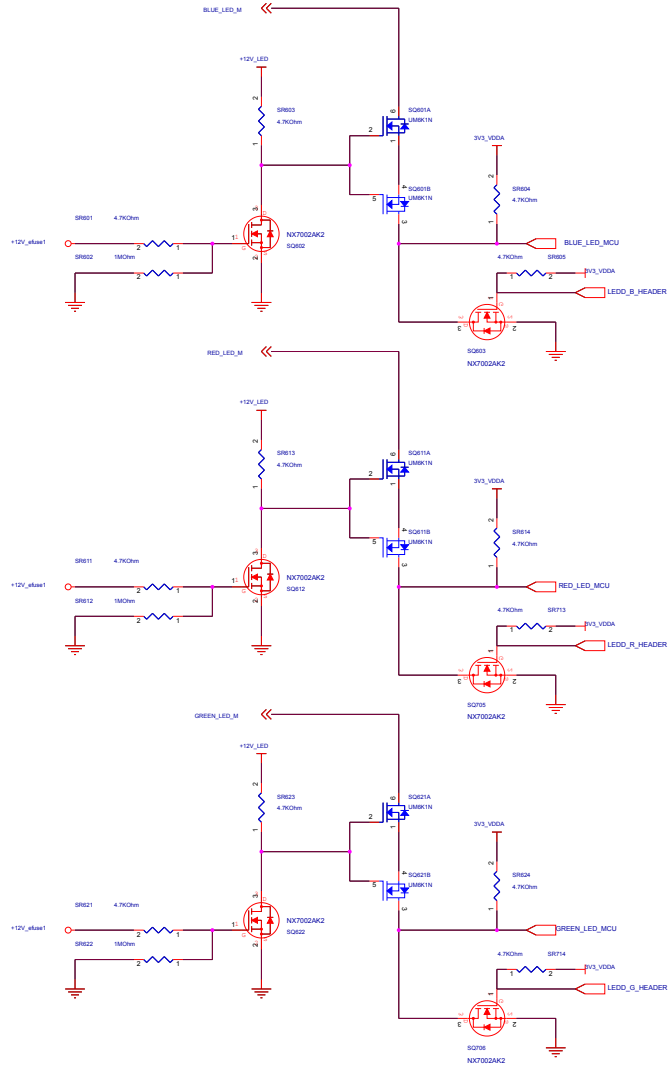


eFuse



限流=2A, (R*3)/10*5 = 1-0.7





+12V_efuse1	LED
12V	HEADER CONTROL
X	MCU CONTROL

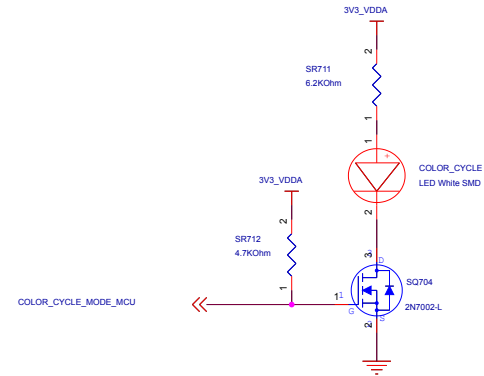
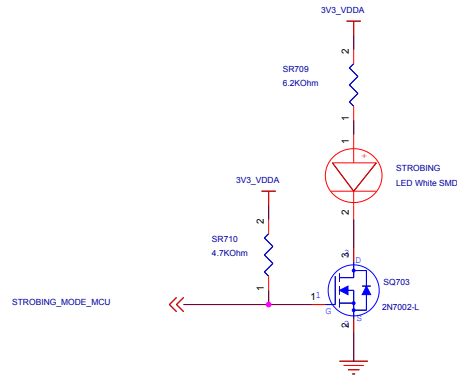
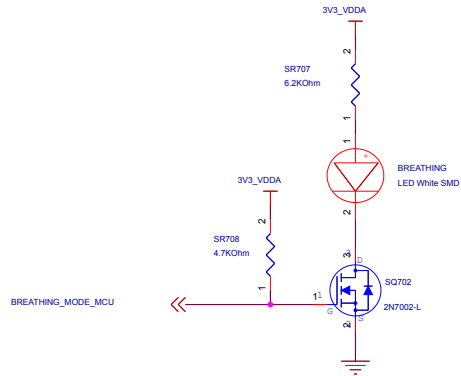
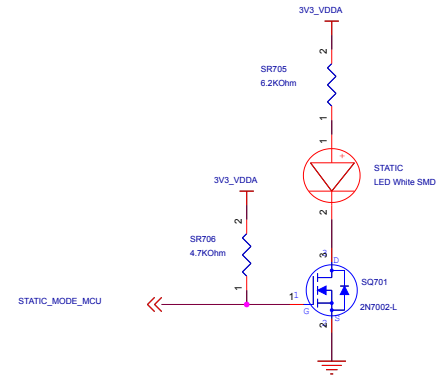
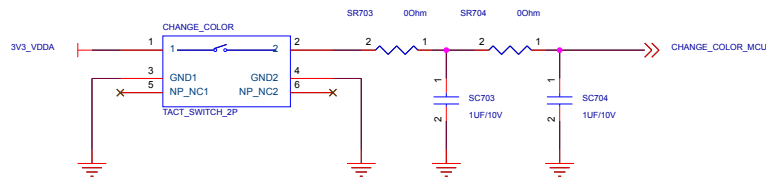
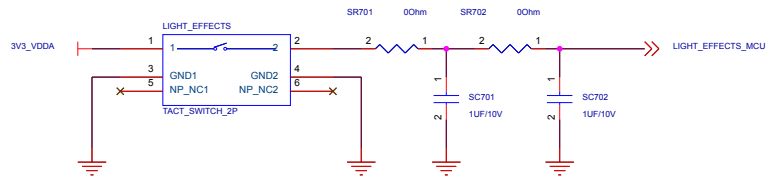


Figure 1 shows four circuit diagrams illustrating different termination configurations for a 100-ohm signal line. Each diagram includes a 5V source, a 100-ohm resistor, and a ground reference (GNDND1).

- Diagram 1 (Top Left):** Shows a 100-ohm resistor (R17862) in series with the signal line, connected to a 5V source and a ground reference (GNDND1). The resistor value is 0Ohm (JX).
- Diagram 2 (Top Right):** Shows a 100-ohm resistor (R17863) in parallel with the signal line, connected to a 5V source and a ground reference (GNDND1). The resistor value is 0Ohm (JX).
- Diagram 3 (Bottom Left):** Shows a 100-ohm resistor (R17864) in parallel with the signal line, connected to a 5V source and a ground reference (GNDND1). The resistor value is 0Ohm (JX).
- Diagram 4 (Bottom Right):** Shows a 100-ohm resistor (R17865) in series with the signal line, connected to a 5V source and a ground reference (GNDND1). The resistor value is 0Ohm (JX).

